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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/784,783	02/24/2004	Yoshinori Shimosakoda	OKI.645	2206

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EXAMINER	
CAO, CHUN	
ART UNIT	PAPER NUMBER
2115	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/784,783	SHIMOSAKODA, YOSHINORI	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,9-12 and 14* is/are rejected.

7)☒ Claim(s) *3,4 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/8/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL REJECTION

1. Claims 1-7 and 9-14 are presented for examination. Claim 8 was canceled.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. The rejections are respectfully maintained to the extended that is applicable to the amended claims and reproduced infra for applicant's convenience.

4. Claims 1, 2, 5-7, 9-12 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Swoboda et al, U.S. patent no. 5,903,746 in view of Applicant Admitted Prior Art (AAPA).

As per claim 1, Swoboda discloses a clock control circuit carrying out control of a clock signal supplied to a central processing unit, the clock control circuit [figures 7, 11] comprising: a high-speed clock source whose oscillation operation is controlled by an operation control signal, and which generates a high-speed clock used in a usual operation mode; a low-speed clock source generating a low-speed clock whose frequency is lower than a frequency of the high-speed clock [col. 8, lines 11-20]; a selector selecting one of the high-speed clock and the low-speed clock in accordance with a selection signal, and outputting the selected one of the high-speed clock and the low-speed clock to the central processing unit; a first control section which, when a standby mode is designated by a mode signal, outputs the operation control signal for stopping the high-speed clock source [see tables 1, 2; col. 7, lines 19-24; col. 8, lines 1-6], and which, when an interrupt signal is supplied, outputs the operation control signal for operating the high-speed clock source; and a second control section which, when

the standby mode is designated by the mode signal, outputs the selection signal for causing the low-speed clock to be selected [col. 6, lines 30-41; col. 7, lines 29-37; col. 9, lines 58-67].

Swoboda fails to explicitly disclose that when the interrupt signal is supplied, starts counting of the low-speed clock, and when a count value reaches a value set in a register, the second control section outputs the selection signal for causing the high-speed clock to be selected.

AAPA discloses when the interrupt signal is supplied, starts counting of the low-speed clock, and when a count value reaches a value set in a register, the second control section outputs the selection signal for causing the high-speed clock to be selected [page 2, lines 1-5; page 2, line 19-page 3, line 5].

It would have been obvious for one of ordinal skill in the art to combine Swoboda and AAPA because they are both directed to a clock control system, and the specify teaching of AAPA would improve the performance and reliability of the Swoboda's system.

As per claim 2, Swoboda discloses an interrupt signal control section which selects an arbitrary one of or plurality of signals from a plurality of interrupt cause signals, and when a cause for interruption arises at any of the selected signals, the interrupt signal control section outputs the interrupt signal [fig. 7; col. 6, lines 31-49].

As per claim 5, Swoboda discloses that the selector includes a two-input OR gate, a two-input AND gate, a flip-flop having a reset input, a low-through latch, and an inverter [fig. 8; col. 7, lines 15-24].

As per claim 6, Swoboda discloses that the high-speed clock source includes an oscillator, and a multiplier which multiplies by a predetermined number the high-speed clock outputted from the oscillator [col. 4, lines 9-27].

As per claim 7, Swoboda discloses that the high-speed clock source includes an oscillator, and a frequency divider which processes the high-speed clock outputted from the oscillator [col. 8, lines 9-19].

As per claim 9, Swoboda discloses that the high-speed clock source is structured so as to be able to select and output one high-speed clock from among a plurality of frequencies [col. 3, lines 15-21].

As per claim 10, AAPA inherently discloses that a comparator which can be connected to an output side of the counter, and a register for setting a value corresponding to a stable time at a time of activation of the high-speed clock source in accordance with a control signal from the central processing unit, wherein the register supplies an output signal to the comparator [page 2, lines 1-5; page 2, line 19-page 3, line 5].

As per claim 11, Swoboda discloses that the flip-flop includes an input signal, a clock input, an asynchronous reset signal, and an output signal, and the low-through latch includes an input signal, a gate control signal, and a gate output, and when the reset input is a first signal, the gate output is reset in accordance with the first signal, and the gate output sets the input signal synchronously with a fall of the clock input [fig. 8; col. 7, lines 15-24].

As per claim 12, Swoboda discloses that the high-speed clock source can generate the high-speed clock, so as to select one frequency from among two or three or more frequencies [col. 3, lines 14-20; col. 8, lines 10-20].

As per claim 14, claim 1 basically is the corresponding elements that are carried out the method of operating steps in claim 14. Accordingly, claims 14 is rejected for the same reason as set forth in claim 1.

Allowable Subject Matter

5. Claims 3, 4 and 13 are rejected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Applicant's arguments with respect to claims 1, 2, 5-7, 9-12 and 14 filed on 1/8/07, which have been fully considered but they are not persuasive.

7. In the remarks, applicants argued in substance that in Applicant's Admitted prior art does not disclose the feature which "when the standby mode is designated by the mode signal, outputs the selection signal for causing the low-speed clock to be selected". In other word, the low-speed clock is provided to the central processing unit during the standby mode.

8. The examiner agreed with applicant position that Applicant's Admitted Prior Art does not disclose the feature. However, Swoboda discloses the feature "when the standby mode is designated by the mode signal, outputs the selection signal for causing the low-speed clock to be selected" [col. 6, lines 30-41; col. 7, lines 29-37; col. 9, lines 58-67; emphasis added, "any one of a large number of clock source can be selected to

optimize the speed of processing for a specific situation such as entering a low power mode (standby mode)"].

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Aoyama, U.S. patent no. 6,763,471, teaches of selecting high-speed clock or low-speed clock for a CPU; when a low power mode is designated by a mode signal, outputs the operation control signal for stopping the high-speed clock source [step S3 in figure 8] when the low power mode is designated by the mode signal, outputs the selection signal for causing the low-speed clock to be selected [step S2 in figure 8] that when the interrupt signal is supplied, starts counting of the low-speed clock [step S4 in figure 8], and when clock count by program processing end, the second control section outputs the selection signal for causing the high-speed clock to be selected [steps S6, S7 in figure 8].

10. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Feb. 13 2007

CHUN CAO
PRIMARY EXAMINER